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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appeal No. _______________

Application No.:	10/804,237
Filing Date:	March 19, 2004
Appellant:	Yonghua Song
Conf. No.:	
Group Art Unit:	2816
Examiner:	Anh Quan Tra
Title:	TEMPERATURE AND PROCESS INDEPENDENT CMOS CIRCUIT

BRIEF ON APPEAL ON BEHALF OF APPELLANTS IN RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

Mail Stop Appeal Brief-Patents
P.O. Box 1450
Alexandria, VA 22313-1450

October 24, 2008

Sir:

This appeal is from the decision of the Patent Examiner dated August 7, 2008 rejecting claims 1-45, 47-56, 58-68, and 70-72, which are reproduced in Appendix A of this Appeal Brief.

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BRIEF ON APPEAL ON BEHALF OF APPELLANT

In support of the Notice of Appeal filed July 11, 2008, appealing the Examiner's Rejection of each of claims 1-45, 47-56, 58-68 and 70-72, mailed April 17, 2008, which appear in the attached Appendix A, Appellant hereby provides the following remarks.

I. REAL PARTY IN INTEREST

The present application is assigned to Marvell International Ltd. as recorded in the Patent and Trademark Office at Reel 010999, Frame 0895 and Reel 010999, Frame 0897 and Reel 011514, Frame 0612.

II. RELATED APPEALS AND INTERFERENCES

The undersigned, the Assignee, and the Appellant do not know of any other appeals or interferences which would directly affect or that would be directly affected by, or have a bearing on, the Board's decision in this Appeal.

III. STATUS OF THE CLAIMS

Claims 1-45, 47-56, 58-68 and 70-72 are reproduced in the attached Appendix A and are the claims on Appeal. Each of these claims is currently pending in the application and is rejected. Claims 46, 57, and 69 are cancelled.

IV. STATUS OF THE AMENDMENTS

There are no pending amendments filed subsequent to a final rejection.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 recites a temperature and process independent analog integrated circuit (See FIG. 4a; Column 6, Lines 22-23) that includes an analog function core (See "analog function circuit," FIG. 4a; Column 6, Lines 23-27) responsive to a first differential input signal and a second differential input signal, and having first and second output terminals. A first loading device (See "RL1," FIG. 4a; Column 6, Lines 30-45) has a first terminal responsive to the first output terminal, a second terminal responsive to a common mode voltage, and a first control terminal. A second loading device (See "RL2," FIG. 4a; Column 6, Lines 30-45) has a third terminal responsive to the second output terminal, a fourth terminal responsive to the common mode voltage, and a second control terminal.

A compensation circuit (See "compensation circuit," FIGS. 4a and 4b; Column 7, Lines 17-29) is in communication with the first and second control terminals. The compensation circuit includes a first MOS transistor (See "M7," FIG. 4b; Column 7, Lines 17-29) having a first source in communication with the common mode voltage, a first drain, and a first gate in communication with the first and second control terminals. A first differential amplifier (See "U2," FIG. 4b; Column 7, Lines 17-29) has a first input in communication with a first bias voltage source, a second input in communication with the first drain, and an output in communication with the first gate and the first and second control terminals.

Independent claim 10 recites a temperature and process independent analog multiplier circuit (See FIG. 4a; Column 6, Lines 22-23) that includes a multiplier core (See "analog function circuit," FIG. 4a; Column 6, Lines 23-27) responsive to a first differential input signal and a second differential input signal, and having first and second output terminals. A first loading device (See "RL1," FIG. 4a; Column 6, Lines 30-45) has a first terminal responsive to the first output terminal, a second terminal responsive to a common mode voltage, and a first control terminal. A second loading device (See "RL2," FIG. 4a; Column 6, Lines 30-45) has a third terminal responsive to

the second output terminal, a fourth terminal responsive to the common mode voltage, and a second control terminal.

A compensation circuit (See "compensation circuit," FIGS. 4a and 4b; Column 7, Lines 17-29) is in communication with the first and second control terminals. The compensation circuit includes a first MOS transistor (See "M7," FIG. 4b; Column 7, Lines 17-29) having a first source in communication with the common mode voltage, a first drain, and a first gate in communication with the first and second control terminals. A first differential amplifier (See "U2," FIG. 4b; Column 7, Lines 17-29) has a first input in communication with a first bias voltage source, a second input in communication with the first drain, and an output in communication with the first gate and the first and second control terminals.

Independent claim 18 recites a temperature and process compensation circuit (See "compensation circuit," FIGS. 4a and 4b; Column 7, Lines 17-29) in communication with control terminals of an active load of an analog integrated circuit (See FIG. 4a; Column 6, Lines 22-23) to counteract changes in an output level of said analog integrated circuit due to temperature and manufacturing process. The temperature and process compensation circuit includes a first MOS transistor (See "M7," FIG. 4b; Column 7, Lines 17-29) having a first source in communication with a common mode voltage, a first drain, and a first gate in communication with the control terminals. A first differential amplifier (See "U2," FIG. 4b; Column 7, Lines 17-29) has a first input in communication with a first bias voltage, a second input in communication with the first drain, and an output in communication with the control terminals. A second MOS transistor (See "M8," FIG. 4b; Column 7, Lines 30-34) has a second gate, a second drain connected to the first drain and a second source. A third MOS transistor (See "M9," FIG. 4b; Column 7, Lines 35-39) has a third gate in communication with a second bias voltage, a third source in communication with a reference point, and a third drain in communication with the second source. A second differential amplifier (See "U1," FIG. 4b; Column 7, Lines 32-41) has a second input connected to the third drain and the second source, a third input in communication with a third bias voltage, and an output in communication with the second gate.

Independent claim 22 recites a temperature and process independent analog integrated circuit (See FIG. 4a; Column 6, Lines 22-23) that includes analog integrated function means (See "analog function circuit," FIG. 4a; Column 6, Lines 23-27) for providing first and second output signals responsive to a first differential input signal pair and a second differential input signal pair. The analog integrated circuit includes first loading means (See "RL1," FIG. 4a; Column 6, Lines 30-45) for providing an output voltage in response to the first output signal, a common mode voltage signal, and a compensation control signal. The analog integrated circuit includes second loading means (See "RL2," FIG. 4a; Column 6, Lines 30-45) for providing an output voltage in response to the second output signal, the common mode voltage signal, and the compensation control signal. The analog integrated circuit includes compensation means (See "compensation circuit," FIGS. 4a and 4b; Column 7, Lines 17-29) for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations.

Independent claim 32 recites a temperature and process independent analog multiplier circuit (See FIG. 4a; Column 6, Lines 22-23) that includes multiplier means (See "analog function circuit," FIG. 4a; Column 6, Lines 23-27) for multiplying a first differential input signal pair and a second differential input signal pair to provide first and second output signals. The analog multiplier circuit includes first loading means (See "RL1," FIG. 4a; Column 6, Lines 30-45) for providing an output voltage in response to the first output signal, a common mode voltage signal, and a compensation control signal. The analog multiplier circuit includes second loading means (See "RL2," FIG. 4a; Column 6, Lines 30-45) for providing an output voltage in response to the second output signal, the common mode voltage signal, and the compensation control signal. The analog multiplier circuit includes compensation means (See "compensation circuit," FIGS. 4a and 4b; Column 7, Lines 17-29) for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations.

Independent claim 41 recites a temperature and process compensation circuit (See "compensation circuit," FIGS. 4a and 4b; Column 7, Lines 17-29) in communication with control terminals of an active load of an analog integrated circuit (See "analog function circuit," FIG. 4a; Column 6, Lines 23-27) to counteract changes in

an output level of said analog integrated circuit due to temperature and manufacturing process. The temperature and process compensation circuit includes a first MOS transistor (See "M7," FIG. 4b; Column 7, Lines 17-29) having a first source in communication with a common mode voltage, a first drain, and a first gate. The circuit includes first differential amplifier means (See "U2," FIG. 4b; Column 7, Lines 17-29) for differentially amplifying a first bias voltage source and a signal from the first drain, and an output, wherein the output of the first differential amplifier means and a signal from the first gate form a compensation control signal.

A second MOS transistor (See "M8," FIG. 4b; Column 7, Lines 30-34) has a second gate, a second drain in communication with the first drain and a second source. A third MOS transistor (See "M9," FIG. 4b; Column 7, Lines 35-39) is in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source. The circuit includes second differential amplifier means (See "U1," FIG. 4b; Column 7, Lines 32-41) for amplifying as a first input the third drain and the second source, and as a second input a third bias voltage source, and to provide output to the second gate.

Independent claim 45 recites an integrated circuit (See FIG. 4a; Column 6, Lines 22-23) that includes an analog function circuit (See "analog function circuit," FIG. 4a; Column 6, Lines 23-27). A differential loading device (See "RL1" and "RL2," FIG. 4a; Column 6, Lines 30-45) is in communication with a differential output of the analog function circuit. A compensation circuit (See "compensation circuit," FIGS. 4a and 4b; Column 7, Lines 17-29) is in communication with the differential loading device. A biasing circuit (See "biasing circuit," FIGS. 4a and 4c; Column 9, Lines 25-26) is in communication with a common mode node of the differential loading device and an input of the compensation circuit. The biasing circuit provides a common mode voltage to the common mode node of the differential loading device and the compensation circuit (See Column 9, Lines 25-34). The common mode voltage is independent of temperature and manufacturing process variations. The biasing circuit provides a plurality of control bias voltage signals to the compensation circuit.

Independent claim 56 recites an integrated circuit (See FIG. 4a; Column 6, Lines 22-23) that includes analog function means for performing an analog function (See

"analog function circuit," FIG. 4a; Column 6, Lines 23-27). The integrated circuit includes differential loading means (See "RL1" and "RL2," FIG. 4a; Column 6, Lines 30-45) for providing a differential load. The differential loading means is in communication with a differential output of the analog function means. The integrated circuit includes compensation means (See "compensation circuit," FIGS. 4a and 4b; Column 7, Lines 17-29) for providing a compensation signal. The compensation means is in communication with the differential loading means.

The integrated circuit includes biasing means (See "biasing circuit," FIGS. 4a and 4c; Column 9, Lines 25-26) for providing a bias signal. The biasing means is in communication with a common mode node of the differential loading means and an input of the compensation means. The biasing means provides a common mode voltage to the common mode node of the differential loading means and the compensation means (See Column 9, Lines 25-34). The common mode voltage is independent of temperature and manufacturing process variations. The biasing means includes means for generating a plurality of control bias voltage signals for the compensation means (See Vcm, Vc1, Vc2, FIG. 4c; Column 9, Lines 25-34).

Independent claim 67 recites a method of performing an analog function (e.g. with an analog integrated circuit shown in FIG. 4a; Column 6, Lines 22-23). The method includes differentially loading the analog function (e.g. with "RL1" and "RL2," FIG. 4a; Column 6, Lines 30-45), providing a common mode node (e.g. Vcm, FIG. 4c; Column 9, Lines 25-34), providing a compensation signal (e.g. Vg, FIG. 4b; Column 7, Lines 17-29), providing a common mode voltage via the common mode node (e.g. with the bias circuit shown in FIG. 4c; Column 9, Lines 25-26), wherein the common mode voltage is independent of temperature and manufacturing process variations, and providing the common mode voltage and a plurality of control bias voltage signals (See Vcm, Vc1, Vc2, FIG. 4c; Column 9, Lines 25-34).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant seeks the Board's review of the rejection of:

(a) claims 1-45, 47-56, 58-68, and 70-72 as being based upon a defective reissue Oath under 35 U.S.C. 251.

VII. ARGUMENTS

A. The Rejections

The rejections that are the subject of this appeal are: a rejection of each of claims 1-45, 47-56, 58-68, and 70-72 as being based upon a defective reissue Oath under 35 U.S.C. 251.

The Examiner alleges that "Applicant has not clearly stated that anything that is listed in the declaration is an error." (See Page 2, Lines 11-12 of the FINAL Office Action mailed April 17, 2008). Further, the Examiner alleges that the "potential ambiguities listed by applicant in the declaration and appear to be editorial in nature and correctable via Certificate of Correction." (See Page 2, Lines 20-21 of the FINAL Office Action mailed April 17, 2008).

B. Oath/Declaration

Appellant respectfully submits that the declaration includes a statement of at least one error which is replied upon to support the reissue application and, as such, the declaration is not in error.

A reissue declaration must contain a statement that the Applicant believes the original patent to be wholly or partly inoperative or invalid by reason of a defective specification or drawing, or by reason of the patentee claiming more or less than patentee had the right to claim in the patent. (MPEP § 1414). Please note that Page 2, Lines 3-4 of Applicant's declaration states "I believe that the original above-identified U.S. patent is partially inoperative by reason of my having claimed less than I had the right to claim in that patent." As such, Appellant respectfully submits that this portion of the requirements for a reissue declaration is satisfied.

Further, a reissue declaration must contain a statement of at least one error which is relied upon to support the reissue application. (MPEP § 1414). Please note that Page 2, Line 4 through Page 3, Line 3 states that a plurality of claims "contain a potential ambiguity with reference to the antecedent basis" for various phrases. The Examiner alleges that "all the potential ambiguities listed by applicant in the declaration appear to be editorial in nature and correctable via Certificate of Correction." Appellant respectfully disagrees and submits that a potential ambiguity due to insufficient antecedent basis is a proper statement of error. In particular, Appellant submits that modification of language intended to eliminate ambiguity is sufficient support for reissue.

Appellant respectfully notes that ambiguity and a lack of antecedent basis can render a claim invalid under 35 U.S.C. § 112, second paragraph. For example, the court in *In re Altenpohl*, 500 F.2d 1151 (C.C.P.A 1974), held that lack of antecedent basis in a claim is proper ground for reissue under 35 U.S.C. § 251:

> lack of antecedent basis in a claim can render it invalid under 35 U.S.C. § 112, second paragraph, and correction of such a defect by issue should not have to depend on difference and scope of claim...a patentee should be allowed to correct an error or ambiguity in a claim without having to rely on implication or litigation. Accordingly, we hold that lack of antecedent basis in claim 11 is proper ground for reissue under 35 U.S.C. § 251. *Id.* at 1156-1157.

In the present declaration, Appellant clearly stated that the error in question is that one or more claims include a potential ambiguity due to improper antecedent basis. As such, Appellant respectfully submits that the declaration is proper. Further, the Examiner has failed to provide any evidence or legal precedent in contradiction of the above holding in *In re Altenpohl*.

For example, in response, the Examiner alleges that Applicant "must state that the specific claim language is ambiguous (i.e., not a potentially ambiguity) and that he believes the ambiguity does render the claim invalid. Just because an ambiguity "can" render the claim invalid does not mean that it does render the claim invalid." (See Page 2, Lines 12-15 of the FINAL Office Action mailed April 17, 2008).

Appellant respectfully disagrees. Initially, please note that the phrase "can render it invalid" is a direct quotation from the above cited case, which held that lack of antecedent basis in a claim **can** render the claim invalid, and that a patentee should be allowed to correct an error or ambiguity in a claim. The Examiner fails to cite any evidence in support of the allegation that there is any meaningful distinction between identifying an *ambiguity* and identifying a *potential ambiguity*. Indeed, Appellant respectfully notes that all ambiguities are inherently "potential" ambiguities because whether or not language is ambiguous is a subjective determination of a future reader.

Here again, a reissue declaration must contain a statement of at least one error. The present reissue declaration clearly identifies multiple errors in the claims that "contain a potential ambiguity with reference to the antecedent basis." In other words, Appellant recognizes and asserts that the claims include language that someone in the future may interpret as ambiguous because of a lack of proper antecedent basis. The Examiner fails to provide any actual evidence that this language is insufficient in view of *In re Altenpohl* or any other legal precedent.

In response, the Examiner merely asserts that "lack of antecedent basis does not automatically render a claim invalid under 35 U.S.C. § 112, 2nd paragraph" and completely ignores Appellant's arguments with respect to *In re Altenpohl* and that court's holding that **lack of antecedent basis in a claim is proper ground for reissue under 35 U.S.C. § 251**. Further, the Examiner fails to provide any evidence whatsoever in support of the allegation that "lack of antecedent basis does not automatically render a claim invalid" and how this relates to Appellant's claims and the holding of *In re Altenpohl*.

In view of the foregoing, Appellant respectfully submits that the declaration contain a statement of at least one error which is relied upon to support the reissue application and claims 1-45, 47-56, 58-68, and 70-72 should be allowable.

VIII. CONCLUSION

Appellant respectfully request the Honorable Board of Patent Appeals and Interferences to reverse the Examiner's rejection of each of pending claims 1-45, 47-56,

58-68, and 70-72. Appellant respectfully submits that the prior art does not teach or suggest one or more limitations of the claims as discussed above. Accordingly, for at least the aforementioned reasons, Appellant respectfully requests the Honorable members of the Board of Patent Appeals and Interferences to reverse the outstanding rejections in connection with the present application and permit each of claims 1-45, 47-56, 58-68, and 70-72 to be passed to allowance in connection with the present application.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Damian M. Aquino, Reg. No. 54,964, at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By: Michael D. Wiggins

Michael D. Wiggins
Reg. No. 34,754

Damian M. Aquino
Reg. No. 54,964

MDW/DMA/rao

Please address all correspondence to:
Harness, Dickey & Pierce, P.L.C.
5445 Corporate Drive
Suite 400
Troy, MI 48098
Customer No. 26703
Tel. No. (248) 641-1600
Fax. No. (248) 641-0270

IX. APPENDIX A

CLAIMS APPENDIX

This is a complete and current listing of the claims.

1. (Original) A temperature and process independent analog integrated circuit comprising:

an analog function core responsive to a first differential input signal and a second differential input signal, and having first and second output terminals;

a first loading device having a first terminal responsive to the first output terminal,

a second terminal responsive to a common mode voltage, and a first control terminal;

a second loading device having a third terminal responsive to the second output terminal, a fourth terminal responsive to the common mode voltage, and a second control terminal; and

a compensation circuit in communication with said first and second control terminals,

wherein said compensation circuit comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate in communication with the first and second control terminals; and

a first differential amplifier having a first input in communication with a first bias voltage source, a second input in communication with the first drain, and an output in communication with the first gate and the first and second control terminals.

2. (Previously Presented) The temperature and process independent analog integrated circuit of claim 1 wherein said analog function core is selected from the group consisting of multipliers, adaptive filters, function generators, modulators, and neural networks.

3. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 1 wherein the analog [integrated] <u>function</u> core [circuit] is a multiplier circuit comprising:

a first current source;

a second current source;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal, a gate of the second MOS transistor in communication with a second terminal of the first differential input signal, commonly connected first drains in communication with the first current source, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal, commonly connected second drains in communication with the second current source, and commonly connected second sources;

a third current source in communication with the commonly connected first sources to form the first output terminal; and

a fourth current source in communication with the commonly connected second sources to form the second output terminal.

4. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 1 wherein the first and second loading devices comprise MOS transistors.

5. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 1 wherein said compensation circuit further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier having a second input in communication with the third drain and the second source, a third input in communication with a third bias voltage source, and an output in communication with the second gate.

6. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 5 wherein the first MOS transistor and the first and second loading devices are of a first conductivity type and the second and third MOS transistors are of a second conductivity type.

7. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 1 further comprising a biasing circuit to provide the common mode voltage to the first and second loading devices.

8. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 5 further comprising a biasing circuit comprising:

a common mode voltage source to provide the common mode voltage that is referenced to a semiconductor bandgap voltage;

a first bias voltage source to provide a first bias voltage to the first MOS transistor that is referenced to the semiconductor bandgap voltage;

a second bias voltage source to provide the second bias voltage to the second MOS transistor that is referenced to a semiconductor bandgap voltage; and

a third bias voltage source to provide the third bias voltage to the third MOS transistor that is referenced to a semiconductor bandgap voltage.

9. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 7 wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

10. (Original) A temperature and process independent analog multiplier circuit comprising:

a multiplier core responsive to a first differential input signal and a second differential input signal, and having first and second output terminals;

a first loading device having a first terminal responsive to the first output terminal, a second terminal responsive to a common mode voltage, and a first control terminal;

a second loading device having a third terminal responsive to the second output terminal, a fourth terminal responsive to the common mode voltage, and a second control terminal; and

a compensation circuit in communication with said first and second control terminals,

wherein said compensation circuit comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate in communication with the first and second control terminals; and

a first differential amplifier having a first input in communication with a first bias voltage source, a second input in communication with the first drain, and an output in communication with the first gate and the first and second control terminals.

11. (Original) The temperature and process independent analog multiplier circuit of claim 10 wherein the multiplier core comprises:

a first current source;

a second current source;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal, a gate of the second MOS transistor in communication with a second terminal of the first differential input signal, commonly connected first drains in communication with the first current source, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal, a gate of the fourth MOS transistor in communication with a

second terminal of the second differential input signal, commonly connected second drains in communication with the second current source, and commonly connected second sources;

a third current source in communication with the commonly connected first sources to form the first output terminal; and

a fourth current source in communication with the commonly connected second sources to form the second output terminal.

12. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 10 wherein the first and second loading devices comprises MOS transistors.

13. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 10 wherein said compensation circuit further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier having a second input in communication with the third drain and the second source, a third input in communication with a third bias voltage source, and an output in communication with the second gate.

14. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 13 wherein the first MOS transistor and the first and second loading devices are of a first conductivity type and the second and third MOS transistors are of a second conductivity type.

15. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 11 further comprising a biasing circuit to provide the common mode voltage to the first and second loading devices.

16. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 13 further comprising a biasing circuit comprising:

a common mode voltage source to provide the common mode voltage that is referenced to a semiconductor bandgap voltage;

a first bias voltage source to provide a first bias voltage to the first MOS transistor that is referenced to the semiconductor bandgap voltage;

a second bias voltage source to provide a second bias voltage to the second MOS transistor that is referenced to a semiconductor bandgap voltage; and

a third bias voltage source to provide a third bias voltage to the third MOS transistor that is referenced to a semiconductor bandgap voltage.

17. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 15 wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

18. (Previously Presented) A temperature and process compensation circuit in communication with control terminals of an active load of an analog integrated circuit to counteract changes in an output level of said analog integrated circuit due to temperature and manufacturing process, said temperature and process compensation circuit comprising:

a first MOS transistor having a first source in communication with a common mode voltage, a first drain, and a first gate in communication with the control terminals;

a first differential amplifier having a first input in communication with a first bias voltage, a second input in communication with the first drain, and an output in communication with the control terminals;

a second MOS transistor having a second gate, a second drain [in communication with] connected to the first drain and a second source;

a third MOS transistor having a third gate in communication with a second bias voltage, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier having a second input connected to the third drain and the second source, a third input in communication with a third bias voltage, and an output in communication with the second gate.

19. (Previously Presented) The temperature and process compensation circuit of claim 18 wherein the first MOS transistor is of [the] a first conductivity type and the second and third MOS transistors are of [the] a second conductivity type.

20. (Previously Presented) The temperature and process compensation circuit of claim 18 further comprising a biasing circuit to provide the common mode voltage and to provide the first bias voltage, second bias voltage, and third bias voltage to said temperature and process compensation circuit.

21. (Previously Presented) The temperature and process compensation circuit of claim 20 further comprising a biasing circuit comprising:

a common mode voltage source to provide the common mode voltage that is referenced to a semiconductor bandgap voltage;

a first bias voltage source to provide [a] the first bias voltage to the first [MOS transistor] differential amplifier that is referenced to the semiconductor bandgap voltage;

a second bias voltage source to provide [a] the second bias voltage to the [second] third MOS transistor that is referenced to a semiconductor bandgap voltage; and

a third bias voltage source to provide [a] the third bias voltage to the [third MOS transistor] second differential amplifier that is referenced to a semiconductor bandgap voltage.

22. (Previously Presented) A temperature and process independent analog integrated circuit comprising:

analog integrated function means for providing first and second output signals responsive to a first differential input signal pair and a second differential input signal pair;

first loading means for providing an output voltage in response to the first output signal, a common mode voltage signal, and a compensation control signal;

second loading means for providing an output voltage in response to the second output signal, the common mode voltage signal, and the compensation control signal; and compensation [circuit] <u>means</u> for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations.

23. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 22 wherein said analog integrated function means is selected from the group consisting of multipliers, adaptive filters, function generators, modulators, and neural networks.

24. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 22 wherein the analog integrated function means is a multiplier circuit comprising:

first current means for supplying a first current; second current means for supplying a second current;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal <u>pair</u>, a gate of the second MOS transistor in communication with a second terminal of the first differential input signal <u>pair</u>, commonly connected first drains responsive to the first current, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal <u>pair</u>, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal <u>pair</u>, commonly connected second drains responsive to the second current, and commonly connected second sources;

third current means for supplying a third current and in communication with the commonly connected first sources to form the first output terminal; and

fourth current means for supplying a third current and in communication with the commonly connected second sources to form the second output terminal.

25. (Previously Presented) The temperature and process independent analog integrated circuit of claim 22 wherein the first and second loading means comprise MOS transistors.

26. (Previously Presented) The temperature and process independent analog integrated circuit of claim 22 wherein said compensation means comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate; and

first differential amplifier means for differentially amplifying a first bias voltage source and a signal from the first drain, wherein an output of the first differential amplifier means and a signal from the first gate form the compensation control signal.

27. (Previously Presented) The temperature and process independent analog integrated circuit of claim 26 wherein said compensation means further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

second differential amplifier means for amplifying as a first input the third drain and the second source, and as a second input a third bias voltage source, and to provide output to the second gate.

28. (Previously Presented) The temperature and process independent analog integrated circuit of claim 27 wherein the first MOS transistor and the first and second loading devices are of [the] a first conductivity type and the second and third MOS transistors are of [the] a second conductivity type.

29. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 22 further comprising biasing means to provide the common mode voltage to the first and second loading means.

30. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 27 further comprising a biasing circuit comprising:

means for generating the common mode voltage that is referenced to a semiconductor bandgap voltage;

means for providing a first bias voltage that is referenced to the semiconductor bandgap voltage;

means for providing a second bias voltage that is referenced to a semiconductor bandgap voltage; and

means for providing a third bias voltage that is referenced to a semiconductor bandgap voltage.

31. (Previously Presented) The <u>temperature and process independent</u> analog integrated circuit of claim 29 wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

32. (Previously Presented) A temperature and process independent analog multiplier circuit comprising:

multiplier means for multiplying a first differential input signal <u>pair</u> and a second differential input <u>signal pair</u> to provide first and second output signals;

first loading means for providing an output voltage in response to the first output signal, a common mode voltage signal, and a compensation control signal;

second loading means for providing an output voltage in response to the second output signal, the common mode voltage signal, and the compensation control signal; and

compensation [circuit] <u>means</u> for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations.

33. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 32 wherein the multiplier means comprises:

first current means for supplying a first current; second current means for supplying a second current;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal pair, a gate of the second MOS transistor in communication with a second terminal of the first differential input signal pair, commonly connected first drains responsive to the first current, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal pair, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal pair, commonly connected second drains responsive to the second current, and commonly connected second sources;

third current means for supplying a third current and in communication with the commonly connected first sources to form the first output terminal; and

fourth current means for supplying a third current and in communication with the commonly connected second sources to form the second output terminal.

34. (Original) The temperature and process independent analog multiplier circuit of claim 32 wherein the first and second loading devices comprises MOS transistors.

35. (Original) The temperature and process independent analog multiplier circuit of claim 32 wherein said compensation means comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate; and

first differential amplifier means for differentially amplifying a first bias voltage source and a signal from the first drain, and an output, wherein the output of the first

differential amplifier means and a signal from the first gate form the compensation control signal.

36. (Original) The temperature and process independent analog multiplier circuit of claim 35 wherein said compensation means further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier means for amplifying as a first input the third drain and the second source, and as a second input a third bias voltage source, and to provide output to the second gate.

37. (Previously Presented) The temperature and process independent analog multiplier circuit of claim [32] 35 wherein the first MOS transistor and the first and second loading devices are of [the] a first conductivity type and the second and third MOS transistors are of [the] a second conductivity type.

38. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 35 further comprising biasing means for providing a common mode voltage to the first and second loading means.

39. (Original) The temperature and process independent analog multiplier circuit of claim 37 further comprising biasing means comprising:

means to generate the common mode voltage that is referenced to a semiconductor bandgap voltage;

means for providing a first bias voltage that is referenced to the semiconductor bandgap voltage;

means for providing a second bias voltage that is referenced to a semiconductor bandgap voltage; and

means for providing a third bias voltage that is referenced to a semiconductor bandgap voltage.

40. (Previously Presented) The temperature and process independent analog [integrated] multiplier circuit of claim 38 wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

41. (Previously Presented) A temperature and process compensation circuit in communication with control terminals of an active load of an analog integrated circuit to counteract changes in an output level of said analog integrated circuit due to temperature and manufacturing process, said temperature and process compensation circuit comprising:

a first MOS transistor having a first source in communication with a common mode voltage, a first drain, and a first gate; and

first differential amplifier means for differentially amplifying a first bias voltage source and a signal from the first drain, and an output, wherein the output of the first differential amplifier means and a signal from the first gate form a compensation control signal;

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier means for amplifying as a first input the third drain and the second source, and as a second input a third bias voltage source, and to provide output to the second gate.

42. (Previously Presented) The temperature and process compensation circuit of claim 41 wherein the first MOS transistor is of [the] a first conductivity type and the second and third MOS transistors are of [the] a second conductivity type.

43. (Previously Presented) The temperature and process compensation circuit of claim 41 further comprising biasing means to provide the common mode voltage and to provide the first bias voltage source, second bias voltage source, and third bias voltage source to said temperature and process compensation circuit.

44. (Previously Presented) The temperature and process compensation circuit of claim 43 wherein said biasing means comprises:

means to generate the common mode voltage that is referenced to a semiconductor bandgap voltage;

means to generate a first bias voltage that is referenced to the semiconductor bandgap voltage;

means to generate the second bias voltage circuit that is referenced to the semiconductor bandgap voltage; and

means to generate the third bias voltage that is referenced to the semiconductor bandgap voltage.

45. (Previously Presented) An integrated circuit, comprising:

an analog function circuit;

a differential loading device in communication with a differential output of the analog function circuit;

a compensation circuit in communication with the differential loading device; and

a biasing circuit in communication with a common mode node of the differential loading device and an input of the compensation circuit,

wherein the biasing circuit provides a common mode voltage to the common mode node of the differential loading device and the compensation circuit, and

wherein the common mode voltage is independent of temperature and manufacturing process variations, and

wherein the biasing circuit provides a plurality of control bias voltage signals to the compensation circuit.

Claim 46 is cancelled.

47. (Previously Presented) The integrated circuit of claim 45, wherein the compensation circuit provides a bias voltage to the differential loading device, and wherein the bias voltage is independent of temperature and manufacturing process variations.

48. (Previously Presented) The integrated circuit of claim 47, wherein the bias voltage varies a differential loading of the differential loading device.

49. (Previously Presented) The integrated circuit of claim 47, wherein the bias voltage is comprised of at least the common mode voltage and the plurality of control bias voltage signals.

50. (Previously Presented) The integrated circuit of claim 47, wherein the bias voltage controls a loading on at least one voltage signal associated with the differential loading device.

51. (Previously Presented) The integrated circuit of claim 47, wherein the differential loading device provides the temperature and process independent output voltage comprised of at least a differential output signal of the analog function circuit, the common mode voltage, and the bias voltage.

52. (Previously Presented) The integrated circuit of claim 45, wherein the plurality of control bias voltage signals are substantially proportional to a semiconductor bandgap voltage.

53. (Previously Presented) The integrated circuit of claim 45, wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

<u>54.</u> (Previously Presented) <u>The integrated circuit of claim 45, wherein the analog function circuit comprises a circuit selected from the group consisting of multipliers, adaptive filters, modulators and neural networks.</u>

<u>55.</u> (Previously Presented) <u>The integrated circuit of claim 45, wherein the differential loading device comprises first and second transistors,</u>

<u>wherein the first transistor comprises a first terminal responsive to a first output terminal of the analog function circuit, a second terminal in communication with the common mode node, and a first control terminal,</u>

<u>wherein the second transistor comprises a third terminal responsive to a second output terminal of the analog function circuit, a fourth terminal in communication with the common mode node, and a second control terminal, and</u>

<u>wherein the biasing circuit is in communication with the first and second control terminals.</u>

<u>56.</u> (Previously Presented) <u>An integrated circuit, comprising:</u>

<u>an analog function means for performing an analog function;</u>

<u>a differential loading means for providing a differential load,</u>

<u>wherein the differential loading means is in communication with a differential output of the analog function means;</u>

<u>a compensation means for providing a compensation signal,</u>

<u>wherein the compensation means is in communication with the differential loading means; and</u>

<u>a biasing means for providing a bias signal,</u>

<u>wherein the biasing means is in communication with a common mode node of the differential loading means and an input of the compensation means,</u>

<u>wherein the biasing means provides a common mode voltage to the common mode node of the differential loading means and the compensation means, and</u>

<u>wherein the common mode voltage is independent of temperature and manufacturing process variations, and</u>

wherein the biasing means comprises means for generating a plurality of control bias voltage signals for the compensation means.

Claim 57 is cancelled.

58. (Previously Presented) The integrated circuit of claim 56, wherein the compensation means comprises means for generating a bias voltage for the differential loading means, and

wherein the bias voltage is independent of temperature and manufacturing process variations.

59. (Previously Presented) The integrated circuit of claim 58, wherein the bias voltage varies a differential loading of the differential loading means.

60. (Previously Presented) The integrated circuit of claim 58, wherein the bias voltage is comprised of at least the common mode voltage and the plurality of control bias voltage signals.

61. (Previously Presented) The integrated circuit of claim 58, wherein the bias voltage controls a loading on at least one voltage signal associated with the differential loading means.

62. (Previously Presented) The integrated circuit of claim 58, wherein the differential loading means provides the temperature and process independent output voltage comprised of at least a differential output signal of the analog function means, the common mode voltage, and the bias voltage.

63. (Previously Presented) The integrated circuit of claim 58, wherein the plurality of control bias voltage signals are substantially proportional to a semiconductor bandgap voltage.

64. (Previously Presented) The integrated circuit of claim 56, wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

65. (Previously Presented) The integrated circuit of claim 56, wherein the analog function means comprises a circuit selected from the group consisting of multipliers, adaptive filters, modulators and neural networks.

66. (Previously Presented) The integrated circuit of claim 56, wherein the differential loading means comprises first and second loading means,

wherein the first loading means comprises a first terminal responsive to a first output terminal of the analog function means, a second terminal in communication with the common mode node, and a first control terminal,

wherein the second loading means comprises a third terminal responsive to a second output terminal of the analog function means, a fourth terminal in communication with the common mode node, and a second control terminal, and

wherein the biasing means is in communication with the first and second control terminals.

67. (Previously Presented) A method of performing an analog function, comprising the steps of:

a.) differentially loading the analog function;

b.) providing a common mode node to step (a.);

c.) providing a compensation signal to step (a.);

d.) providing a common mode voltage to step (a.) via the common mode node, wherein the common mode voltage is independent of temperature and manufacturing process variations; and

e.) providing the common mode voltage and a plurality of control bias voltage signals to step (c.).

68. (Previously Presented) The method of claim 67, wherein step (c.) further comprises the step of

f.) providing a bias voltage to step (a.),

wherein the bias voltage is independent of temperature and manufacturing process variations.

69. (Cancelled).

70. (Previously Presented) The method of claim 67, wherein the compensation signal provided by step (c.) varies the differential loading of step (a.).

71. (Previously Presented) The method of claim 67, wherein the plurality of control bias voltage signals are substantially proportional to a semiconductor bandgap voltage.

72. (Previously Presented) The method of claim 67, wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

X. APPENDIX B

EVIDENCE APPENDIX

A copy of the Final Office Action mailed April 17, 2008 is attached.

XI. APPENDIX C

RELATED PROCEEDINGS APPENDIX

A pre-appeal brief was previously filed with respect to the present application. In response to the appeal brief, the Examiner issued the Notice of Panel Decision mailed August 7, 2008.